B: Amendments to The Claims:

1. (Currently Amended) A method for providing an area optimized binary orthogonality checker ~~for a scalable selector system for controlling data transfers and routing in a data processing system~~ comprising the steps of:

determining ~~the~~ a logical gate count for an implementation of an optomized orthogonality checker for a scalable selector system for controlling data transfers and routing in a data processing system; and minimizing the logical gate count and an implementation of said orthogolality checker given a library of logical gates to implement a minimized circuit and ~~the~~ given an area for each logical gate in the library and to optomize an hierarchical orthogonality structure for said hierarchical design of said circuit while maintaining a hierarchical design for a circuit.

2 (Currently Amended) The method according to claim 1 including the steps of: establishing an optimal mix of hierarchical level; and determining ~~the~~ inputs to implement said orthogonality checker for said minimized circuit.

3. Currently Amended) The method according to claim 1, where the area of said orthogonality checker is implemented in ~~a~~ static CMOS circuits by minimizing the logical gate count and an area needed for checker implementation given a library of logical gates to implement the circuit and the area ~~for~~ of each gate in the library.

4. (Previously Amended) The method according to claim 3, including a step of establishing an optimal mix of hierarchical levels and inputs to implement said orthogonality checker to achieve said minimized circuit.

5. (Previously Amended) The method according to claim 4 wherein said orthogonality checker is employed in a scalable selector system for controlling date transfers and routing in a data processing system, comprising a plurality of input data buses coupled to a multiple-bit, multiple bus selector having data, data valid, and an outputs of orthogonality checker and having multiple data input bus ports coupled for receipt of signal from said plurality of input data buses.

6. (Currently Amended) A method employed in a data processing system having a plurality of input data buses coupled to a multiple-bit, multiple bus selector having data, data valid, and outputs of an orthogonality checker and having multiple data input bus ports coupled for receipt of signal from said plurality of input data buses comprising the steps of:

establishing an expected number for a logical gate count ~~for~~ of an implementation of an orthogonality checker, and providing binary orthogonality checking by hierarchically combining the outputs of said orthogonality checker with smaller numbers of inputs and by performing ~~the~~ a total check of a large number of inputs with less gates and in a smaller area.

7. (Currently Amended) The method according to claim 6 wherein after determining an expected number for the logical gate count, then providing multiple checks are combined with reduced input sets ~~are combined~~ into one larger check and orthogonality checking is performed, with a check on each input set, as well as with combining an OR of all the inputs for providing resulting OR values to the one larger check.

8. (Currently Amended) The method according to claim 7 wherein the resulting OR values are then checked for orthogonality, and ~~the~~ results of all the checks are Ored together.

9. (Currently Amended) The method according to claim 8 wherein said orthogonality checker is extended to multiple hierarchical levels and works with orthogonality checks for an extended size of implementation.

10. (Previously Amended) The method according to claim 9 wherein the orthogonality checker has an optimal hierarchical structure for a given technology library and a given number of inputs to check.